Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix[[;]],

wherein at least one of the memory cells ~~including~~ comprises:

a memory thin film transistor; and

a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating surface;

~~a first insulating film;~~

a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween; and

~~a second insulating film;~~

a control gate electrode adjacent to the floating gate with a second insulating film therebetween,

wherein said switching thin film transistor ~~including~~ comprises:

a second semiconductor active layer over the insulating surface; and

~~a gate insulating film;~~

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the first semiconductor active layer ~~of the memory thin film transistor~~ and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor, and

wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask

~~wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and~~

~~wherein the second insulating film comprises a thermal oxide film of the floating gate electrode~~.

2-76. (Canceled)

77. (Currently Amended) A semiconductor device comprising:

a substrate;

a non-volatile memory over the substrate;

a pixel portion over the substrate;

a source wiring driver circuit for driving the pixel portion over the substrate;

a gate wiring driver circuit for driving the pixel portion over the substrate; and

a correction circuit over the substrate,

wherein the non-volatile memory comprises a plurality of memory cells,

wherein at least one of the memory cells comprises:

a memory thin film transistor; and

a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating surface; ~~a first insulating film;~~

a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween;

~~a second insulating film;~~ and

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating surface;

~~a gate insulating film;~~ and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the first semiconductor active layer ~~of the memory thin film transistor~~ and the second semiconductor active layer are in a common semiconductor island, and

wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask.

78. (Currently Amended) A semiconductor device comprising:

a substrate;

a non-volatile memory over the substrate;

a pixel portion;

a source wiring driver circuit for driving the pixel portion over the substrate;

a gate wiring driver circuit for driving the pixel portion over the substrate; and

a memory controller circuit over the substrate for controlling the non-volatile memory circuit,

wherein the non-volatile memory comprises a plurality of memory cells,

wherein at least one of the memory cells comprises:

a memory thin film transistor; and

a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating surface ~~a first insulating film~~;

a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween;

~~a second insulating film;~~ and

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating surface;

~~a gate insulating film;~~ and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the first semiconductor active layer ~~of the memory thin film transistor~~ and the second semiconductor active layer are in a common semiconductor island, and

wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask.

79. (Currently Amended) A semiconductor device comprising:

a substrate;

a non-volatile memory over the substrate;

a pixel portion over the substrate;

a source wiring driver circuit for driving the pixel portion over the substrate;

a gate wiring driver circuit for driving the pixel portion over the substrate; and

a correction circuit over the substrate,

wherein the non-volatile memory comprises a plurality of memory cells,

wherein at least one of the memory cells comprises:

a memory thin film transistor; and

a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating surface; ~~a first insulating film;~~

a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween;

~~a second insulating film;~~ and

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating surface;

~~a gate insulating film;~~ and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the first semiconductor active layer ~~of the memory thin film transistor~~ and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor, and

wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask.

80. (Currently Amended) A semiconductor device comprising:

a substrate;

a non-volatile memory over the substrate;

a pixel portion;

a source wiring driver circuit for driving the pixel portion over the substrate;

a gate wiring driver circuit for driving the pixel portion over the substrate; and

a memory controller circuit over the substrate for controlling the non-volatile memory circuit,

wherein the non-volatile memory comprises a plurality of memory cells,

wherein at least one of the memory cells comprises:

a memory thin film transistor; and

a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating surface; ~~a first insulating film;~~

a floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween;

~~a second insulating film;~~ and

a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating surface;

~~a gate insulating film;~~ and

a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the first semiconductor active layer ~~of the memory thin film transistor~~ and the second semiconductor active layer are in a common semiconductor island, ~~and~~

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor, and

wherein a channel forming region in the first semiconductor active layer is formed by a self-aligning manner using the floating gate as a mask.

81. (Previously Presented) A semiconductor device according to claim 77,

wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.

82. (Previously Presented) A semiconductor device according to claim 78,

wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.

83. (Previously Presented) A semiconductor device according to claim 79,

wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.

84. (Previously Presented) A semiconductor device according to claim 80,

wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.

85-86. (Canceled)

87. (Previously Presented) A device according to claim 77,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

88. (Previously Presented) A device according to claim 78,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

89. (Previously Presented) A device according to claim 79,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

90. (Previously Presented) A device according to claim 80,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

91-92. (Canceled)

93. (Previously Presented) A device according to claim 77,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

94. (Previously Presented) A device according to claim 78,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

95. (Previously Presented) A device according to claim 79,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

96. (Previously Presented) A device according to claim 80,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

97. (Previously Presented) A nonvolatile memory according to claim 1, wherein the first and the second semiconductor active layers contain amorphous silicon germanium.

98. (Previously Presented) A device according to claim 77, wherein the first and the second semiconductor active layers contain amorphous silicon germanium.

99. (Previously Presented) A device according to claim 78, wherein the first and the second semiconductor active layers contain amorphous silicon germanium.

100. (Previously Presented) A device according to claim 79, wherein the first and the second semiconductor active layers contain amorphous silicon germanium.

101. (Previously Presented) A device according to claim 80, wherein the first and the second semiconductor active layers contain amorphous silicon germanium.

102. (New) A nonvolatile memory according to claim 1, wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.